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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/829,114	04/09/2001	Hajime Kimura	SEL 249	2293

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EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 06/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/829,114	KIMURA, HAJIME	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-37,39-61 and 63-70* is/are pending in the application.

4a) Of the above claim(s) *4,6,7,15-34,37,39,40,42-56,59-61,63-65 and 67-70* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8-14,35,36,41,57 and 66* is/are rejected.

7)☒ Claim(s) *58* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/09/01,06/10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 04/15/2005 have been fully considered but they are not persuasive. The Examiner acknowledges the Applicant's effort in making claims 1-3,8-14,35,36,41,57,58 and 66 allowable by incorporating the limitation of claims 5, 38, 62 into independent claims 1, 35 and 57 respectively. However, after further consideration, it is the Examiner's position that these claims are not allowable, and this will be discussed in detail by the following rejections to the claims. The Examiner apologizes for any inconvenience this may cause the Applicant.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 8, 9, 35, 36, 41, 57 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, Ohzu et al. (US PG-PUB # 2002/0167601) and in further view of Houston (US Patent # 5,917,365).

[Claim 1]

Applicant's admitted prior art teaches a semiconductor device (figure 8) comprising an amplifying transistor (801), a biasing transistor (802), an amplifying side power source line (803); a biasing side power source line (804); a bias signal line (802). Applicant's admitted prior art discloses in figure 8 a drain terminal of the amplifying transistor being connected to the amplifying side power source line (803), a source terminal of the biasing transistor is connected

to the biasing side power source line (804), a source terminal of the amplifying transistor (801) is connected to a drain terminal of the biasing transistor, a gate terminal (V_b) of the biasing transistor (802) is connected to the bias signal line, a gate terminal of the amplifying transistor (801) serves as an input terminal (V_{in}), and a source terminal of the amplifying transistor (801) serves as an output terminal (V_{out}, Paragraphs 24 and 25)

Applicant's admitted prior art fails to teach an electric discharging transistor and an electric discharging power source line wherein one of the output terminal and the electric discharging power source line is connected to a source terminal of the electric discharging transistor while the other thereof is connected to a drain terminal of the electric discharging transistor.

However Ohzu et al. teaches an electric discharging transistor (figure 5, element 38-1) and an electric discharging power source line wherein the output terminal is connected to a power source line and the electric discharging power source line is connected to a drain terminal of the electric discharging transistor (38-1) in order to charge/discharge the capacitor (Paragraph 186).

Therefore taking the combined teachings of Applicant's admitted prior art and Ohzu, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have an electric discharging transistor and an electric discharging power source line wherein one of the output terminal and the electric discharging power source line is connected to a source terminal of the electric discharging transistor while the other thereof is connected to a drain terminal of the electric discharging transistor. The benefit of doing so would be reduce image lag or after image as compared to conventional case as taught in Ohzu (Paragraph 186).

Applicant's admitted prior art in view of Ohzu fail to teach wherein an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

However Houston teaches that the threshold voltage of a transistor is the minimum voltage that must be applied to the gate of the transistor in order for the transistor to "turn on"; otherwise the transistor is "turned off" (col. 1 lines 28-32) and therefore reads on an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

Therefore taking the combined teachings of Applicant's admitted prior art, Ohzu and Houston it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state in order to have high performance and low standby current.

[Claim 2]

Applicant's admitted prior art teaches a load capacitance (805) wherein one terminal of the load capacitance is connected to the output terminal (V_{out}), and the other terminal of the load capacitance is connected to a load capacitance power source line (806).

[Claim 3]

Ohzu teaches the electric discharging power source line (37-1) is connected to the biasing side power source line (36-1)..

[Claim 8]

Applicant's admitted prior art teaches an area sensor having plurality of pixels with one biasing transistor for one output line (Paragraph 11, figure 3, output line 303). Therefore for a plurality of output lines corresponding to plurality of pixels there with be plurality of biasing transistors. Houston teaches that the threshold voltage of a transistor is the minimum voltage that must be applied to the gate of the transistor in order for the transistor to "turn on"; otherwise the transistor is "turned off" (col. 1 lines 28-32).

[Claim 9]

The combination of applicant's admitted prior art and Ohzu teach that the amplifying transistor (801), the biasing transistor (802), and the electric discharging transistor (37-1) are transistors having the same polarity (same symbols).

[Claims 35 and 57]

These are method claims corresponding to apparatus claim 1 wherein the discharging transistor (37-1) as taught in Ohzu et al. will be used to perform a discharge inherently only when the discharging transistor is in a conductive state.

[Claim 36]

This is a method claim corresponding to apparatus claim 2. Therefore it has been analyzed and rejected based upon apparatus claim 2.

[Claim 41]

This is a method claim corresponding to apparatus claim 8. Therefore it has been analyzed and rejected based upon apparatus claim 8.

[Claim 66]

See claim 9.

4. Claims 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art , Ohzu et al. (US PG-PUB # 2002/0167601), Houston (US Patent # 5,917,365) and in further view of Silver et al. (US Patent # 6,690,842).

[Claims 10-14]

Applicant's admitted prior art , Ohzu et al. and Houston teaches the limitations of claim 1. Ohzu et al. teaches that the semiconductor device can be used in a camera (Also read as a computer or portable communication terminal, Paragraph 5) but fails to teach other devices like X-ray and a scanner. However Silver et al. teaches that for forming digital images a number of devices like a digital camera , line-scan scanners, X-ray devices such as CT scanners can be used (col. 1 lines 15-20). Therefore taking the combined teachings of Applicant's admitted prior art , Ohzu et al., Houston and Silver, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to use the semiconductor device of Ohzu into other devices like X-ray and a scanner. The benefit of doing so would be a reduction in cost of manufacture because the same imaging sensor might be used in a number of devices.

Allowable Subject Matter

5. Claim 58 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: As for claim 58, the prior art fails to teach or suggest fairly wherein a value of an electric potential of the electric discharging power source line takes a value that is between an electric potential of the bias signal line and an electric potential of the biasing side power source line.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
June 20, 2005

DAVID L. OMETZ
PRIMARY EXAMINER